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Modeling and Simulation Of Three Phase-Four Wire Compensated System Using The H-Bridge VSI Topology-Based DSTATCOM

N UDAY BHANU[1], B.SHANKAR PRASAD[2]

1student, Department of EEE,St.Theressa college, Visakhapatnam- 530 045
2Assistance Professor,HOD, Department of EEE, St.Theressa college, Visakhapatnam- 530 045

Abstract—The Transient response of the distribution static compensator (DSTATCOM) is very important while compensating rapidly varying unbalanced and nonlinear loads. Any change in the load affects the dc link voltage directly. The sudden removal of load would result in an increase in the dc link voltage above the reference value where as a sudden increase in the load would reduce the dc link voltage below its reference value. The proper operation of DSTATCOM requires variation of the DC link voltage within the prescribed limits. Conventionally, a proportional-integral (PI) controller is used to maintain the dc-link voltage to the reference value. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional PI dc-link voltage controller is slow. In this paper, a fast acting dc-link voltage controller based on the energy of the dc-link capacitor is proposed and proposed shunt controller method by using PQ-Theory. Mathematical equations are given to compute the gains of the conventional controller based on the fast-acting dc-link controllers to achieve similar fast transient response. The detailed simulation studies are carried out to validate the proposed controller.

Index Terms—DC-link voltage controller, distribution static compensator (DSTATCOM), fast transient response, harmonics, load compensation, power factor, power quality, unbalance and voltage-source inverter (VSI) , PQ-Theory.

I. INTRODUCTION

The proliferation of the power electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power quality (PQ) problems in the power distribution network. They cause excessive neutral currents, over heating of electrical apparatus, poor power factor, voltage distortion, and high levels of neutral –to-ground voltage, and inference with communication systems. The literature records the evolution of different custom power devices to mitigate the power-quality problems by injecting the voltages/currents or both in to the system.

The shunt connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it.

One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature to compute the reference compensator currents. However, due to simplicity in formulation and no confusion regarding the definition of powers, the control algorithm based on instantaneous symmetrical component theory is preferred. Based on algorithm, compensator reference currents ($i_{fa}^*, i_{fb}^*, i_{fc}^*$) are given as follows:

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \{(v_{sa} + \gamma(v_{sb} - v_{sc}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \\ i_{fb}^* &= i_{lb} - \{(v_{sb} + \gamma(v_{sc} - v_{sa}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \\ i_{fc}^* &= i_{ic} - \{(v_{sc} + \gamma(v_{sa} - v_{sb}))(P_{lavg} + P_{dc})/(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\} \end{aligned}\right\} \longrightarrow (1)$$

Where γ=tanφ/√3 and φ is the desired phase angle between the supply voltages and compensated source currents in the respective phases. For unity power factor operation, φ=0, thus γ=0. The term P_{lavg} is the dc or average value of the load power. The term P_{dc} in the above equations accounts for the losses in the VSI without any dc loads in its dc

link. To generate P_{dc}, a suitable closed loop dc link voltage controller should be used, which will regulate the dc voltage to the reference value.

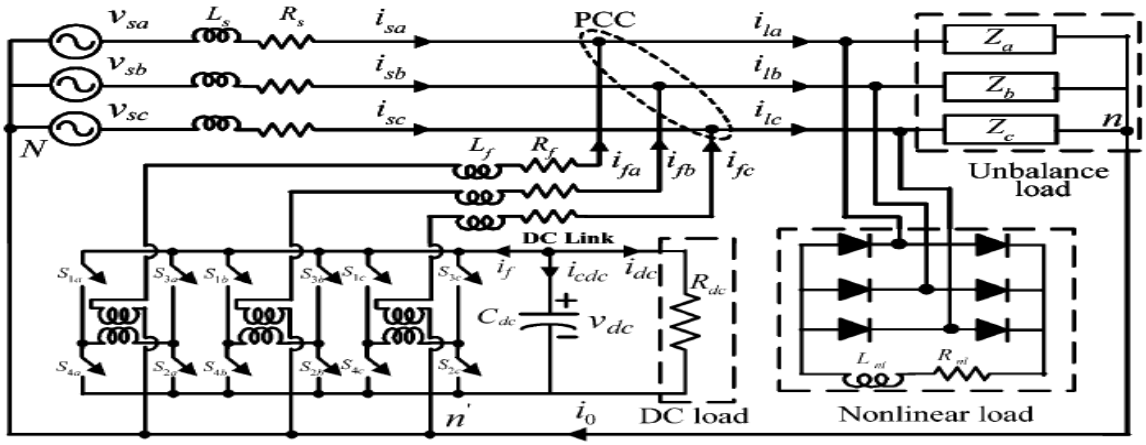
For the DSTATCOM compensating unbalanced and nonlinear loads, the transient performance of the compensator is decided by the computation time of average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of average load power. Therefore, the transient performance of the compensator mostly depends on the computation of P_{lavg}. In this paper, P_{lavg} is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics present in voltages and currents. Although the computation of P_{dc} is generally slow and updated once or twice in a cycle, being a small value compared to P_{lavg} it does not play a significant role in transient performance of the compensator.

In some of the electric power consumers, such as the telecommunication industry, power electronic drive applications there is a requirement for ac as well as dc loads. The telecommunication industry uses several parallel-connected switch-mode rectifiers to support dc bus voltage. Such an arrangement draws nonlinear load currents from the utility. This causes poor power factor and hence more losses and less efficiency. Clearly, there are PQ issues, such as unbalance, poor power factor, and harmonics produced by telecom equipment in power distribution networks. Therefore, the functionalities of the conventional DSTATCOM should be increased to mitigate aforementioned PQ problems and to supply the dc loads from its dc link as well. The load sharing by the ac and dc bus depends up on the design and rating of VSI. This DSTATCOM differs from the conventional one in the sense that its dc link not only supports instantaneous compensation but also supplies dc loads.

However, when the dc link of the DSTATCOM supplies the dc load as well, the corresponding dc power is comparable to the average load power and hence plays a major role in the transient response of the compensator. Hence there are two important issues. The first one is the regulation of the dc link voltage with prescribed limits under transient load conditions. The second one is the settling time of the dc link voltage controller. Conventionally, a PI controller is used to maintain the dc link voltage. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional dc-link voltage controllers is slow especially in the applications where the load changes rapidly. Some work related to the dc link voltage controllers and their stability is reported in [16]-[20]. However work is limited to rectifier units where switching patterns are well defined and analysis can be easily carried out. In this paper, a fast acting dc link voltage controller based on dc link capacitor energy is proposed. The detailed modeling, simulation and experimental verifications are given to prove the efficacy of this fast acting dc link voltage controller. There is no systematic procedure to design the gains of the conventional PI controller used to regulate the dc link voltage of the DSTATCOM. Herewith, mathematical equations are given to design the gains of the conventional controller based on the fast acting dc link voltage controller to achieve similar fast transient response.

II. DSTATCOM FOR COMPENSATING AC AND DC LOADS

Various VSI topologies are described in the literature for realizing the DSTATCOM to compensate unbalanced and nonlinear loads [21]-[29]. Due to the simplicity, the absence of the unbalance in the dc link voltage and independent current tracking with respect to other phases, a three phase H-Bridge VSI topology is chosen. The following figure.1: shows a three phase-four-wire-compensated system using H-bridge VSI topology-based DSTATCOM compensating unbalanced and nonlinear ac load.



(Figure.1: showing a three phase-four wire compensated system using the H-bridge VSI topology-based DSTATCOM)

A dc load (R_{dc}) is connected across the dc link. The DSTATCOM consists of 12 insulated-gate bipolar transistor(IGBT) switches each with an antiparallel diode, dc strorage capacitor, three isolation transformers and three interface conductors.The statr point of the isolation transformers(n') is connected to the neutral of load(n) and source (N). The H-bridge VSIs are connected to the PCC through interface inductors. The isolation transformers prevent a short circuit of the dc capacitor for various combinations of switching states of the VSI. The inductance and resistance of the isolation transformers are also included in L_f and R_f. The source voltages are assumed to be balanced and sinusoidal. With this supply being considered as a stiff source, the feeder impedance(L_s-R_s) shown in the above figure.1: is negligible and hence it is not accounted in state-space modelling. To track the desired compensator currents, the VSIs operate under the hysterisis band current control mode due to their simplicity, fast response, and being independent of the load parameters [30]. The DSTATCOM injects currents in to the PCC in such a way as to cancel unbalance and harmonics in the load currents. The VSI operation is supported by the dc storage capacitor C_{dc} with voltage V_{dc} across it. The dc bus voltage has two functions, that is, to support the compensator operationand to supply dc load. While compensating, the DSTATCOM mantains the balanced sinusoidal source currents with unity power factor and supplies the dc load through its dc bus.

III. STATE-SPACE MODEL OF THE DSTATCOM

For the DSTATCOM topology shown in the above Figure.1: the pairs of switches S_{1a}-S_{2a} and S_{4a}-S_{3a} are always ON and OFF in complimentary mode. The ON and OFF states of these switches are represented by a binary logic variable S_a and its complement$\bar{S}_a$. Thus when switches S_{1a}-S_{2a} are ON, it implies that switches S_{4a}-S_{3a} are OFF. This is represented by S_a=1, $\bar{s}_a$=0, and vice-versa. In a similar wayS_b ,$\bar{S}_b$ and S_c & $\bar{S}_c$ represent gating signals for switches S_{1b}-S_{2b},S_{4b}-S_{3b},S_{1c}-S_{2c},S_{4c}-S_{3c}, respectively. Using the notations for the system shown in the above figure the state-space equations are written as follows:

$\dot{\mathbf{x}}$ = **Ax** + **Bu** ——————————————————————————▶ (2)

Where state vector **x** and input vector **u** are given by

x =[i_{fa} i_{fb} i_{fc} v_{dc}] T (3)

u = [v_{sa} v_{sb} v_{sc}] T ——————————————————————▶ (4)

here **T** is the transpose operator.

System matrix [**A]** and input matrix [**B**] are given as follows:

$$\mathbf{A} = \begin{bmatrix} -R_f/L_f & 0 & 0 & (S_a - \bar{S}_a)/L_f \\ 0 & -R_f/L_f & 0 & (S_b - \bar{S}_b)/L_f \\ 0 & 0 & -R_f/L_f & (S_c - \bar{S}_c)/L_f \\ -(S_a - \bar{S}_a)/C_{dc} & -(S_b - \bar{S}_b)/C_{dc} & -(S_c - \bar{S}_c)/C_{dc} & -1/R_{dc}C_{dc} \end{bmatrix} \longrightarrow (5)$$

$$\mathbf{B} = \begin{bmatrix} 1/L_f & 0 & 0 \\ 0 & 1/L_f & 0 \\ 0 & 0 & 1/L_f \\ 0 & 0 & 0 \end{bmatrix} \longrightarrow (6)$$

Using the above state-space model, the system state variables (**x**) are computed at every instant.

IV. DC-LINK VOLTAGE CONTROLLERS

As mentioned before, the source supplies an unbalanced nonlinear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in figure.1. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc link voltage, closed-loop controllers are used. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as

$$u_c = K_p(V_{dcref} - v_{dc}) + K_i\int (V_{dcref} - v_{dc})\, dt + K_d\, \mathrm{d}\,(V_{dcref} - v_{dc})/dt \longrightarrow \quad (7)$$

In (7), K_p, K_i and K_d are proportional, integral and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain (K_p) reduces rise time and steady-state error but increase the overshoot and settling time. An increase in integral gain (K_i) reduces steady-state error but increases overshoot and settling time. Increasing derivative gain (K_d) will lead to improved stability. However practitioners have often found that the derivative term can behave against anticipatory action in case of transport delay. A cumbersome trail-and-error to tune its parameters made many practitioners switch-off or even exclude the derivative term [31], [32]. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following sections.

A. Conventional DC- Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in figure.2. To maintain the dc link voltage at the reference value, the dc link capacitor needs a certain amount of real power, which is proportional to the difference between actual and reference voltages. The power required by the capacitor can be expressed as follows:

$$P_{dc} = K_p(V_{dcref} - v_{dc}) + K_i\int (V_{dcref} - v_{dc})\, dt. \longrightarrow (8)$$

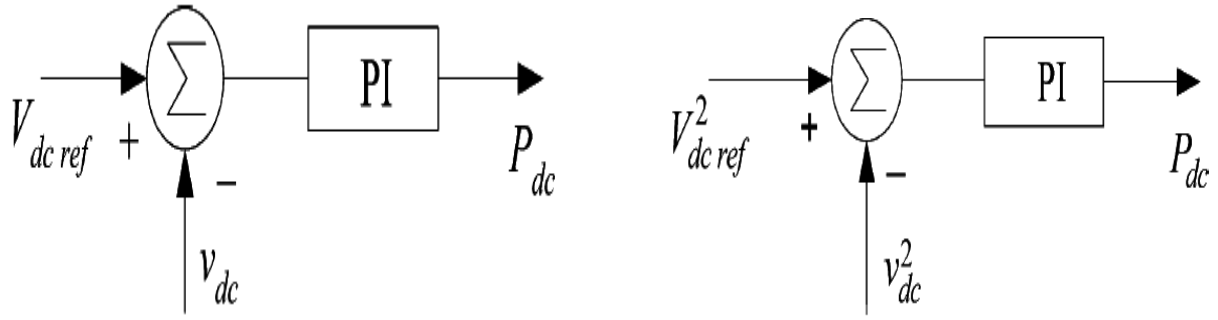


Figure.2. Schematic diagram of the conventional dc-link voltage controller

Figure.3. Schematic diagram of the fast-acting dc-link voltage controller

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase a supply voltage. The sampling can also be performed at a quarter-cycle depending up on the symmetry of the dc link voltage wave form. The drawback of this conventional controller is that its transient response is slow, especially for fast changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of K_p and K_i when P_{dc} is comparable toP_{lavg}.

B. Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc link capacitor (W_{dc}) to charge from actual voltage (v_{dc}) to the reference value (V_{dcref}) can be computed as

$$W_{dc} = ½C_{dc}(V_{dcref}^2 - v_{dc}^2). \longrightarrow (9)$$

In general, the dc link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc power (P'_{dc}) required by the dc link capacitor is given as

$$P'_{dc} = W_{dc}/T_c = (1/2T_c)C_{dc}(V_{dcref}^2 - v_{dc}^2) \longrightarrow (10)$$

Where T_c is the ripple period of the dc link capacitor voltage, some control schemes have been reported in [33] and [34].However, due to the lack of integral term, there is a steady-state error while compensating the combined ac and dc loads. This is eliminated by including the integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages. This controller is shown in figure.3 and the total dc power required by the dc link capacitor is computed by the following equation:

$$P_{dc} = K_{pe}(V_{dcref}^2 - v_{dc}^2) + K_{ie}\int (V_{dcref}^2 - v_{dc}^2)dt. \longrightarrow (11)$$

The coefficients K_{pe} and K_{ie} are proportional and integral gains of the proposed energy-based dc-link voltage controller. Energy based controller gives fast response compared to the conventional PI controller. Thus, it can be called a fast acting dc link voltage controller. The ease in the calculation of the proportional and integral gains is an additional advantage. The value of the proportional controller gain K_{pe} can be given as

$$K_{pe} = C_{dc}/2T_c \longrightarrow (12)$$

For example, if the value of dc link capacitor is 2200μF and the capacitor voltage ripple period is 0.01 s, then K_{pe} is computed as 0.11 by using (12). The selection of K_{ie} depends up on the tradeoff between the transient response and overshoot in the compensated source current. Once this proportional gain is selected, integral gain is changed around and chosen to be 0.5. It is found that if K_{ie} is greater than$\frac{K_{pe}}{2}$, the response tends to be oscillatory and if K_{ie} is less than$\frac{K_{pe}}{2}$, then response tends to be sluggish. Hence, K_{ie} is chosen to be$\frac{K_{pe}}{2}$.

V. DESIGN OF CONVENTIONAL CONTROLLER BASED ON THE FAST-ACTING DC-LINK VOLTAGE CONTROLLER

The conventional dc-link voltage controller can be designed based on equations given for the fast-acting dc-link voltage controller as in (11) and can be written as

$$P_{dc} = K_{pe}(V_{dcref} + v_{dc})(V_{dcref} - v_{dc}) + K_{ie}\int (V_{dcref} + v_{dc})(V_{dcref} - v_{dc})dt. \longrightarrow (13)$$

It can also be written as

$$P_{dc} = K'_p(V_{dcref} - v_{dc}) + K'_i\int (V_{dcref} - v_{dc})dt. \longrightarrow (14)$$

Where

$K_p' = K_{pe}(V_{dcref} + v_{dc})$ ⟶ (15)

$K_i' = K_{ie}(V_{dcref} + v_{dc})$ ⟶ (16)

It is observed from the aforementioned equations that the gains of proportional and integral controllers vary with respect to time. However, for small ripples in the dc-link voltage, $v_{dc} \approx V_{dcref}$

Therefore, we can approximate the above gains to the following:

$K_p' \approx 2K_{pe}(V_{dcref})$ ⟶ (17)

$K_i' \approx 2K_{ie}(V_{dcref})$ ⟶ (18)

The relations (17) – (18) give approximate gains for a conventional PI controller. This is due to the fact that $(V_{dcref} + v_{dc})$ is not really equal to $2V_{dcref}$ until variation of v_{dc} is small during transients. Hence, the designed conventional PI controller works only on approximation. The open-loop gains for the two cases are given by

$P_{dc}/E_{er} = (K_{pe}(s + K_{ie}/K_{pe}))/s$ ⟶ (19)

Where $E_{er} = V_{dcref}^2 - v_{dc}^2$ and

$P_{dc}/E_{er} = K_p'(s + \frac{K_i'}{K_p'})/s$ ⟶ (20)

Where $E_{er} = (V_{dcref} - v_{dc})$. Since $\frac{K_i'}{K_p'}$ is same as K_{ie}/K_{pe} and the higher gain in the conventional PI controller renders less stability than that of the proposed energy-based dc-link controller. For the same performance, the conventional PI controller has gains which are 364(40/0.11 from table 1) times larger than that of the proposed one. Also, the amplifier units used to realize these gains need more design considerations and are likely to saturate when used with higher gains.

TABLE 1
SIMULATION PARAMETERS:

System Parameters	Values
Supply voltage	400 V (L-L), 50 Hz
Unbalanced Load	Z_a = 25 Ω, Z_b = 44 + j25.5 Ω and Z_c = 50 + j86.6 Ω
Nonlinear Load	Three-phase full wave rectifier drawing a dc current of 5 A
DC Load	R_{dc} = 100 Ω
DC capacitor	C_{dc} = 2000 µF
Interface Inductor	L_f = 26 mH, R_f = 0.25 Ω
Reference dc link voltage	V_{dcref} = 520 V
Hysteresis band	±h = 1.0 A
Gains of conventional dc link voltage controller	K_p = 40, K_i = 20
Gains of fast-acting dc link voltage controller	K_p = 0.11, K_i = 0.055

VI. SELECTION OF THE DC-LINK CAPACITOR

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in figure.1 is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by X × 1000J/s. Let us further assume that the compensator deals with

half (that is X/2) and twice (that is 2X) capacity under the transient conditions for n cycles with the system voltage period of T s. Then, the change in energy to be with by the dc capacitor is given as

$\Delta E = (2X - X/2)nT$ ⟶ (21)

Now this change in energy (21) should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-link voltage from 1.4 V_m to 1.8 V_m during the transient conditions where V_m is the peak value of the phase voltage. Hence we can write

$\frac{1}{2} C_{dc}[(1.8V_m)^2 - (1.4V_m)^2] = (2X-X/2)nT$ ⟶ (22)

$\Rightarrow C_{dc} = 3XnT/[(1.8V_m)^2 - (1.4V_m)^2]$ ⟶ (23)

For example, consider a 10-KVA system (with X = 10 KVA), peak voltage V_m = 352.2 V, n = 0.5, and T = 0.02s. The value of C_{dc} computed using (23) is 2216 µF. In practical 2000 µF is readily available and the same value has been for simulation and experimental studies.

VII.PROPOSED SHUNT CONTROLLER METHOD USING PQ-THEORY

The control algorithm for series active power filter (APF) is based on unit vector template generation scheme , where as the control strategy for shunt APF is discussed in this section. Based on the load on the 3P4W system, the current drawn from the utility can be unbalanced. In this paper a new control strategy is proposed to compensate the current unbalance present in the load currents by expanding the concept of single phase p—q theory (28), (29). According to this theory, a signal phase system can be defined as a pseudo two-phase system giving π/2 lead or π/2 lag, that is each phase voltage and current of the original three-phase system can be considered as three independent two phase systems. These resultant two phase systems can be represented in α—β coordinates, and thus, the p—q theory applied for balanced three phase system can also be used for each phase of unbalanced system independently. The actual load voltages and load currents are considered as α—axis quantities where as the π/2 lead load or π/2 lag voltages and π/2 lead or π/2 lag load currents are considered as β—axis quantities. In this paper π/2 lead is considered to achieve a two phase system for each phase. The major advantage of p—q theory is that it gives poor results under distorted and/or unbalanced input/utility voltages . In order to eliminate these limitations, the reference load voltage signals extracted for series APF are used instead of actual load voltages.

For phase a, the load voltage and current in α—β coordinates can be represented by π/2 lead as

$$\begin{bmatrix} v_{La\_\alpha} \\ v_{La\_\beta} \end{bmatrix} = \begin{bmatrix} v^*_{La}(\omega t) \\ v^*_{La}(\omega t + \frac{\pi}{2}) \end{bmatrix} = \begin{bmatrix} v_{Lm}\sin(\omega t) \\ v_{Lm}\cos(\omega t) \end{bmatrix} \longrightarrow (24)$$

$$\begin{bmatrix} i_{La\_\alpha} \\ i_{La\_\beta} \end{bmatrix} = \begin{bmatrix} i_{La}(\omega t + \varphi L) \\ i_{La}[(\omega t + \varphi L) + \frac{\pi}{2}] \end{bmatrix} \longrightarrow (25)$$

Where $v^*_{La}(\omega t)$ represents the reference load voltage and v_{Lm} represents the desired load voltage magnitude. Similarly for phase b, the load voltage and current in α—β coordinates can be represented by π/2 lead as,

$$\begin{bmatrix} v_{Lb\_\alpha} \\ v_{Lb\_\beta} \end{bmatrix} = \begin{bmatrix} v^*_{Lb}(\omega t) \\ v^*_{Lb}(\omega t + \frac{\pi}{2}) \end{bmatrix} = \begin{bmatrix} v_{Lm}\sin(\omega t - 120°) \\ v_{Lm}\cos(\omega t - 120°) \end{bmatrix} \longrightarrow (26)$$

$$\begin{bmatrix} i_{Lb\_\alpha} \\ i_{Lb\_\beta} \end{bmatrix} = \begin{bmatrix} i_{Lb}(\omega t + \varphi L) \\ i_{Lb}[(\omega t + \varphi L) + \frac{\pi}{2}] \end{bmatrix} \longrightarrow (27)$$

In addition for phase c, the load voltage and current in α—β coordinates can be represented by π/2 lead as

$$\begin{bmatrix} v_{Lc\_\alpha} \\ v_{Lc\_\beta} \end{bmatrix} = \begin{bmatrix} v_{Lc}^{*}(\omega t) \\ v_{Lc}^{*}(\omega t + \frac{\pi}{2}) \end{bmatrix} = \begin{bmatrix} v_{Lm}\sin(\omega t + 120°) \\ v_{Lm}\cos(\omega t + 120°) \end{bmatrix} \longrightarrow (28)$$

$$\begin{bmatrix} i_{Lc\_\alpha} \\ i_{Lc\_\beta} \end{bmatrix} = \begin{bmatrix} i_{Lc}(\omega t + \varphi L) \\ i_{Lc}[(\omega t + \varphi L) + \frac{\pi}{2}] \end{bmatrix} \longrightarrow (29)$$

By using the definition of three phase p—q theory, for balanced three-phase system (3), the instantaneous power components can be represented as
Instantaneous active power

$$p_{L,abc} = v_{L,abc\_\alpha} \cdot i_{L,abc\_\alpha} + v_{L,abc\_\beta} \cdot i_{L,abc\_\beta} \cdot \longrightarrow (30)$$

Instantaneous reactive power

$$q_{L,abc} = v_{L,abc\_\alpha} \cdot i_{L,abc\_\beta} - v_{L,abc\_\beta} \cdot i_{L,abc\_\alpha} \cdot \longrightarrow (31)$$

Considering the phase a, the phase-a instantaneous load active and instantaneous load reactive powers can be represented by

$$\begin{bmatrix} p_{La} \\ q_{La} \end{bmatrix} = \begin{bmatrix} v_{La\_\alpha} & v_{Lb\_\beta} \\ -v_{Lb\_\beta} & v_{La\_\alpha} \end{bmatrix} \longrightarrow (32)$$

Where

$$p_{La} = \bar{p}_{La} + \tilde{p}_{La} \longrightarrow (33)$$

$$q_{La} = \bar{q}_{La} + \tilde{q}_{La} \longrightarrow (34)$$

In (33) and (34), $\bar{p}_{La}$ and $\bar{q}_{La}$ represent the DC components that are responsible for fundamental load active and reactive powers, whereas $\tilde{p}_{La}$ and $\tilde{q}_{La}$ represent the ac components that are responsible for harmonic powers. The phase-a fundamental instantaneous load active and reactive power components can be extracted from p_{La} and q_{La}, respectively by using a low pass filter.
Therefore, the instantaneous fundamental load active power for phase-a is given by

$$p_{La,1} = \bar{p}_{La} \longrightarrow (35)$$

And Instantaneous fundamental load reactive power for phase-a is given by

$$q_{La,1} = \bar{q}_{La} \longrightarrow (36)$$

Similarly the fundamental instantaneous load active and the fundamental instantaneous load reactive powers for phases-b and c can be calculated as
Instantaneous fundamental load active power for phase b

$$p_{Lb,1} = \bar{p}_{Lb} \longrightarrow (37)$$

Instantaneous fundamental load reactive power for phase b

$$q_{Lb,1} = \bar{q}_{Lb} \longrightarrow (38)$$

Instantaneous fundamental load active power for phase c

$$p_{Lc,1} = \bar{p}_{Lc} \longrightarrow (39)$$

Instantaneous fundamental load reactive power for phase c

$$q_{Lc,1} = \bar{q}_{Lc} \longrightarrow (40)$$

Since the load current drawn by each phase may be different due to different loads that may be present inside plant, therefore the instantaneous fundamental load active power and the instantaneous fundamental load reactive power demand for each phase may not be the same. In order to make this load unbalanced power demand, seen from the utility side, as a perfectly balanced fundamental three phase active power, the unbalanced load power

should be properly redistributed between utility, UPQC and load such that the total load seen by the utility would be linear and balanced load. The unbalanced or balanced reactive power demanded by the load should be handled by a shunt APF. The aforementioned task can be achieved by summing instantaneous load active power demands of all the three phases and redistributing it again on each utility phase that is from equations (35), (37) and (39).

$$p_{L,Total} = p_{La,1} + p_{Lb,1} + p_{Lc,1} \longrightarrow (41)$$

$$p^*_{S/ph} = (p_{L,Total})/3 \longrightarrow (42)$$

Equation (42) gives the distributed per phase fundamental active power demand that each phase of utility should supply in order to achieve perfectly balanced source currents. From (42) it is evident that under all the conditions the total fundamental active power demand by the loads would be equal to the total power drawn from the utility but with perfectly balanced way even though the load currents are unbalanced. Thus the reference compensating currents representing a perfectly balanced three-phase system can be extracted by taking the inverse of (32).

$$\begin{bmatrix} i^*_{Sa\_\alpha} \\ i^*_{Sa\_\beta} \end{bmatrix} = \begin{bmatrix} v_{La\_\alpha} & v_{La\_\beta} \\ -v_{La\_\beta} & v_{La\_\alpha} \end{bmatrix}^{-1} \cdot \begin{bmatrix} p^*_{S/ph} + p_{dc/ph} \\ 0 \end{bmatrix} \longrightarrow (43)$$

In (43), $p_{dc/ph}$ is the precise amount of per-phase active power that should be taken from the source in order to maintain the dc-link voltage at a constant level and to overcome the losses associated with UPQC, The oscillating instantaneous active power $\tilde{p}_{La}$ should be exchanged between the load ad shunt APF. The reactive power term q_{La} in (43) is considered as zero since the utility should not supply load reactive power demand. In the above matrix, the α-axis reference compensating current represents the current that is at $\frac{\pi}{2}$lead with respect to the original system.

Therefore, $i^*_{Sa}(t) = \{v_{La\_\alpha}(t)/(v^2_{La\_\alpha} + v^2_{La\_\beta})\} . \{p^*_{\underline{S}}(t) + p^*_{dc/ph}(t)\}$ ⟶ (44)

Similarly the reference source currents for phases b and can be estimated as

$$i^*_{Sb}(t) = \{v_{Lb\_\alpha}(t)/(v^2_{Lb\_\alpha} + v^2_{Lb\_\beta})\} . \{p^*_{\underline{S}}(t) + p^*_{dc/ph}(t)\} \longrightarrow (45)$$

$$i^*_{Sc}(t) = \{v_{Lc\_\alpha}(t)/(v^2_{Lc\_\alpha} + v^2_{Lc\_\beta})\} . \{p^*_{\underline{S}}(t) + p^*_{dc/ph}(t)\} \longrightarrow (46)$$

The reference neutral current signal can be extracted by simply adding all the sensed load currents without actual neutral current sensing as

$$i_{L\_n}(t) = i_{La}(t) + i_{Lb}(t) + i_{Lc}(t) \longrightarrow (47)$$

$$i^*_{Sh\_n}(t) = -i_{L\_n}(t). \longrightarrow (48)$$

The proposed balanced per-phase fundamental active power estimation, dc link voltage control based on PI regulator, the reference neutral current generation are shown in
figures A:(a) and (d) respectively.

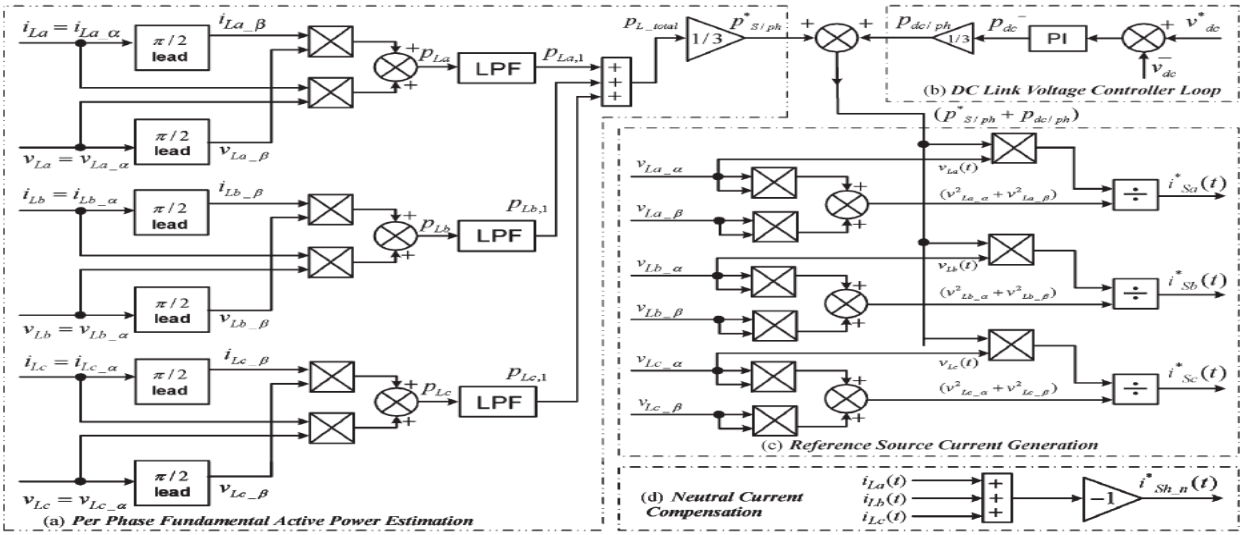


Figure.A. Shunt active filter control block diagram. (a) Proposed balanced per-phase fundamental active power estimation. (b) DC-link voltage control loop. (c) Reference source current generation. (d) Neutral current compensation.

VIII. SIMULATION STUDIES

The load compensator with H-bridge VSI topology as shown in figure.1 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the PCC. The ac load consists of a three phase unbalanced load and a three phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance (R_{dc}) as shown in the figure. The dc load forms 50% of the total power requirement. The system and compensator parameters are given in table1.

By monitoring the load currents and PCC voltages, the average load power is computed. At every zero crossing of phase a voltage, P_{dc} is generated by using the dc-link voltage controller. The state space equations are solved to compute the actual compensator currents and dc-link voltage. These actual currents are compared with the reference currents given by (1) using hysteresis current control. Based on the comparison, switching signals are generated to compute the actual state-variables by solving the state-space model given in (2). The source voltages and load currents are plotted in figure 4(a) and (b).

The load currents have total harmonic distortions of 8.9%, 14.3%, and 21.5% in phases a, b and c, respectively. The unbalance in load currents results in neutral current as illustrated in the figure.

The compensator currents and compensated source currents are shown in Figure 4© and (d). As seen from figure 4(d), the source currents are balanced sinusoids; however, the switching frequency components are superimposed over the reference currents due to the switching action of VSI. The currents have a unity power factor relationship with voltages in the respective phases. The THDs in

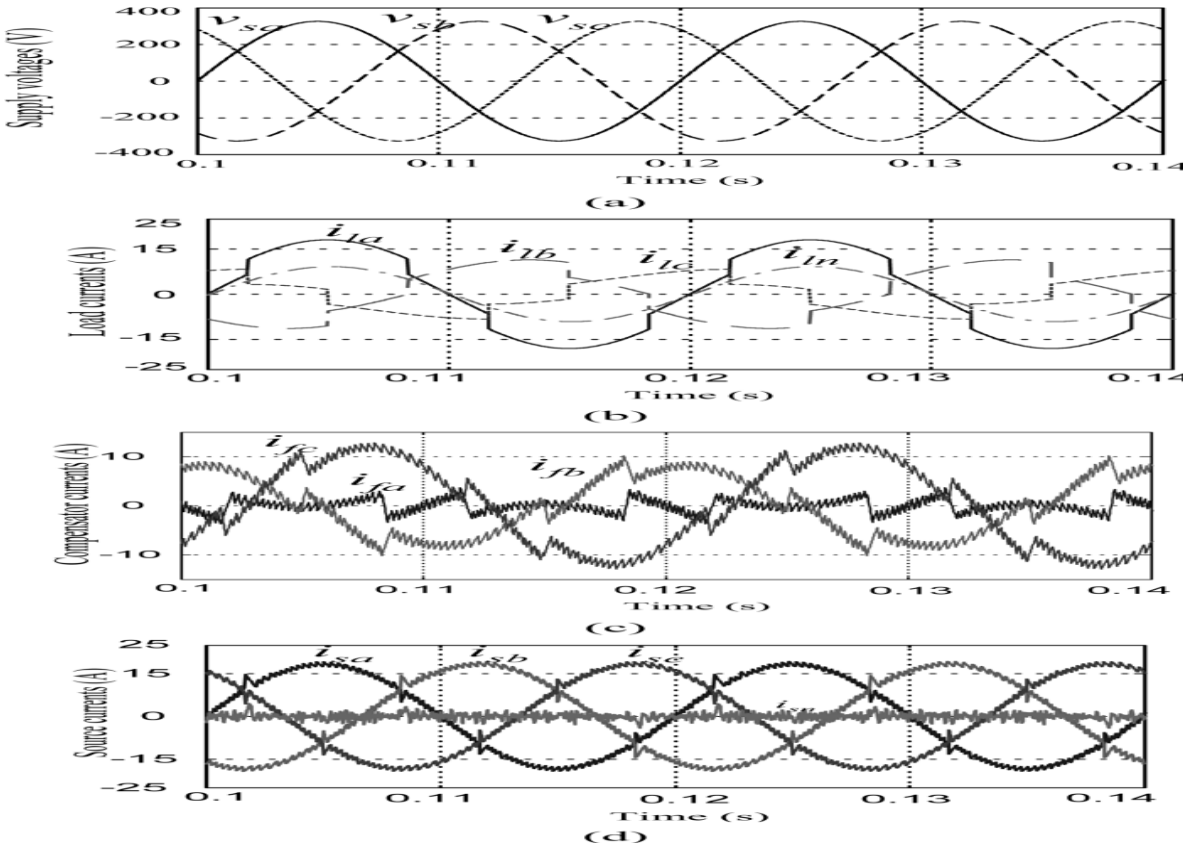


Figure 4 (a) supply voltages (b) Load currents (c) Compensator currents (d) Compensated source currents.

These currents are 3.6%, 3.7% and 3.9% in phases a, b and c respectively. There are notches in the source currents due to finite bandwidth of VSI. The transient performance of the conventional and fast acting dc link voltage controllers are studied by making sudden changes in the ac load supplied by the ac load bus as well as the dc load supplied by the dc link. In the simulation study, the load is halved at the instant t = 0.4s and brought back to full load at t = 0.8s. The transient performance is explained in the subsections.

A. Transient Performance of Conventional DC-Link Voltage Controller

The conventional dc-link voltage controller as given in (8) is used to generate the dc load power P_{dc} which is inclusive of losses in the inverter. The transient performance of the compensator is shown in figure 5(a) and (b). The total load, which is a combination of linear unbalanced and nonlinear load (as given in table 1), is halved at the instant t = 0.4s. Due to a sudden reduction in the load, the dc link capacitor absorbs surplus power from the source. Therefore, there is an increase in dc link capacitor voltage above the reference value. Based on the values of PI controller will be brought back to the reference value after a few cycles.

Similarly, when the load is switched back to the full load at instant t = 0.8s, the dc capacitor supplies power to the load momentarily and hence the dc link voltage falls below the reference value. Due to the PI controller action, the capacitor voltage will gradually build up and reach its reference value. If gains of the conventional dc link voltage would have undesirable overshoot and considerably large settling time. Consequently, the performance of the load connected to the dc link also gets affected due to the above factors. It can be observed from figure 5(a) and (b) that the conventional dc link voltage controller takes about a ten cycle period to reach the reference voltage during load transient. This is indicated by time duration t_s in these figures

.

B. Transient Performance of Fast-Acting DC-Link Voltage Controller

The dc load power P_{dc} is computed by using the fast acting dc link voltage controller as given in (11). Transients in the load are considered the same as in the above simulation study. Figure 6(a) and (b) illustrates the phase a source current and dc link capacitor voltage during the load transients.

At the instant t = 0.4s, the capacitor voltage increases due to the sudden removal of the load. The fast acting dc link voltage controller takes action at instant t = 0.41s. This is because the controller output is updated at every half-cycle. It computes the dc load power P_{dc} needed to bring the capacitor voltage to the reference value in a half-cycle. Therefore, the dc link voltage reaches its reference voltage at the instant t = 0.42s. When the dc link voltage is more than the reference value, P_{dc} is less. Therefore, the source currents are less in magnitude.

At the instant t = 0.8s, the dc link voltage falls below the reference voltage due to a sudden increase in load. As explained earlier, the fast acting controller brings the dc link voltage to its reference value at t = 0.82s with almost the same rise in voltages as that of the conventional dc link voltage controller. A close observation of the figure would reveal that the fast acting dc link voltage controller can regulate the capacitor voltage with in half-cycle period which is indicated byt_s. Owing to its good transient performance, it is preferred over the conventional dc link voltage controller.

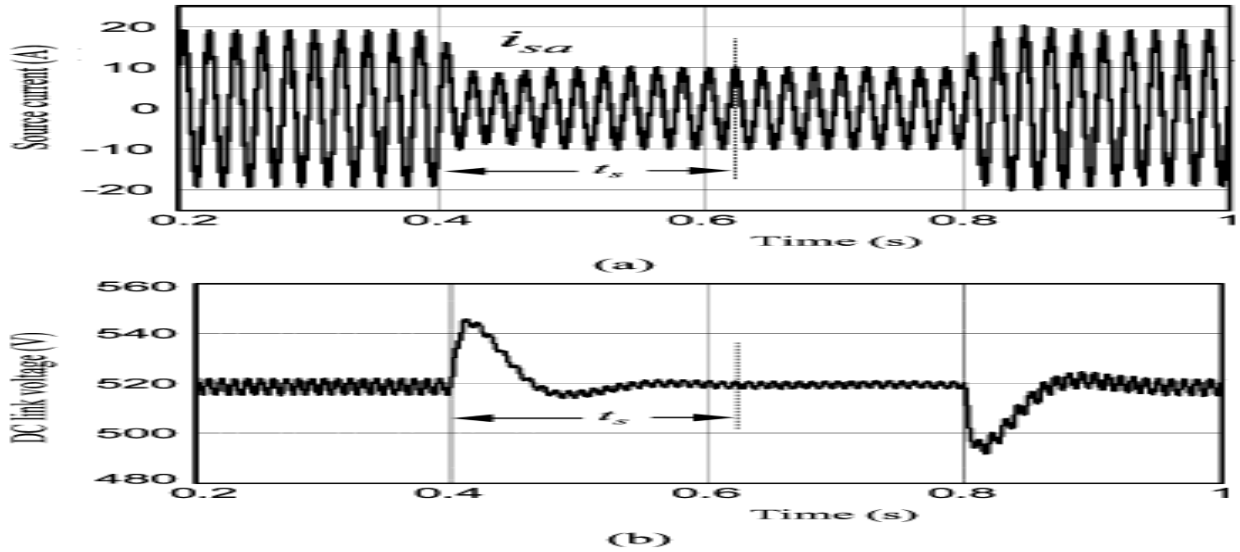


Figure5: Transient response of the conventional controller. (a) Compensated source current in phase a. (b) DC-Link voltage.

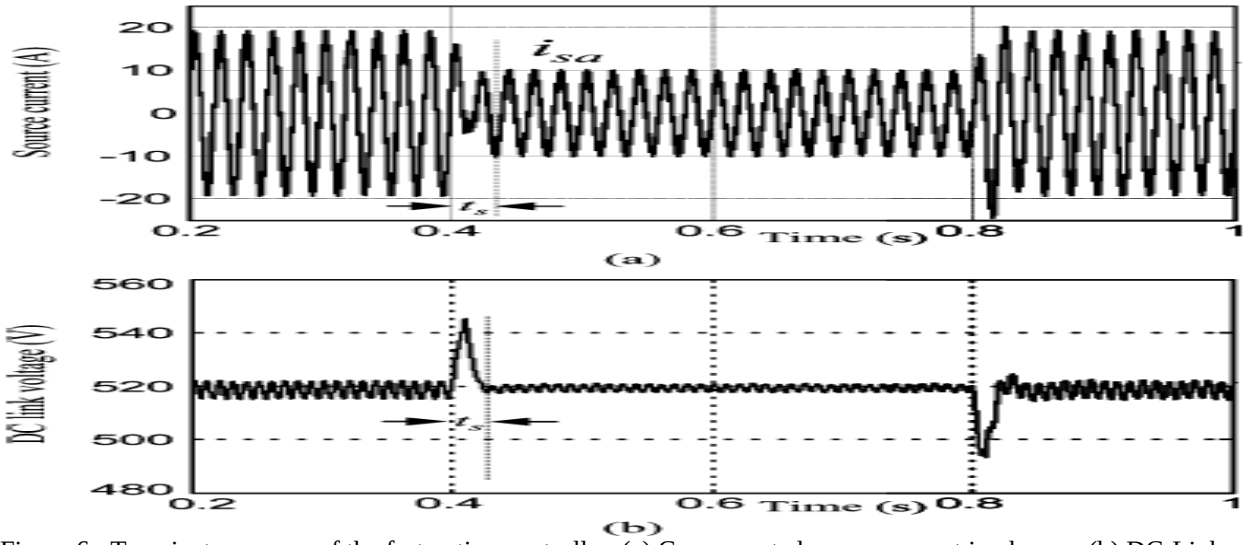


Figure 6: Transient response of the fast-acting controller. (a) Compensated source current in phase a. (b) DC-Link voltage.

IX.PROPOSED METHOD SIMULATION RESULTS:

The average load power is computed by taking samples of the load currents and PCC voltages. The dc load power (P_{dc}) is generated by using the conventional dc link voltage controller and fast acting dc link voltage controllers. Based on these values, reference compensator currents are obtained by using (1). The VSI is then operated in the hysteresis band current control mode to synthesize the actual compensator currents. Accordingly, the switching commands are issued to control IGBT switches through proper interfacing circuits.

The source voltages and load currents are shown in figure 8(a) and (b), respectively. The source voltages are balanced and sinusoidal but the load currents have both unbalance and distortions. The unbalance in load currents results in neutral current. The THDs of the load currents are 11.6%, 16.7% and 24.2% in phases a, b and c respectively. Compensator and compensated source currents are shown in figure 8 (c) and (d) respectively. The source currents are balanced sinusoids with the THDs of 5.2%, 4.8% and 4.7% in phases a, b and c respectively.

A.Transient Performance of the Conventional DC-Link Voltage Controller

The transient performance with the conventional dc link voltage controller is shown in figure.9. At the instant t =t_1, the unbalanced linear R-L load and a half dc load are removed. At t = t_2 the load is brought to its original value. The power (P_{dc}) required by the dc link is computed by using (8). Figure 9 illustrates the compensated source currents and dc link voltage. From this figure, it can be understood that the usage of the conventional controller with an improper value of controller gains cannot bring the actual dc link voltage to its reference value quickly. It takes around 40 cycles to regulate the dc link voltage to its reference voltage.

B.Transient Performance of the Fast-Acting DC-Link Voltage Controller

The performance of the fast acting dc link voltage controller is tested by using the trandsient load used in the previous section. Figure 10 shows the source currents during the transients in load by using this fast acting dc link voltage controller as given in (11). From the close observatoion of the figure, it is found that the response time is very less compared to that of the conventional dc link voltage controller. Though, in simulation studies, the fast acting voltage controller corrects the actual dc link voltage in a half cycle, the experimental results do not fully validate the same. This is due to the use of the mechanical switch for the change of load, which can not connect/disconnect the load in all three phases simultaneously at the instants t_1 and t_2 and due to other nonidealities in the system.

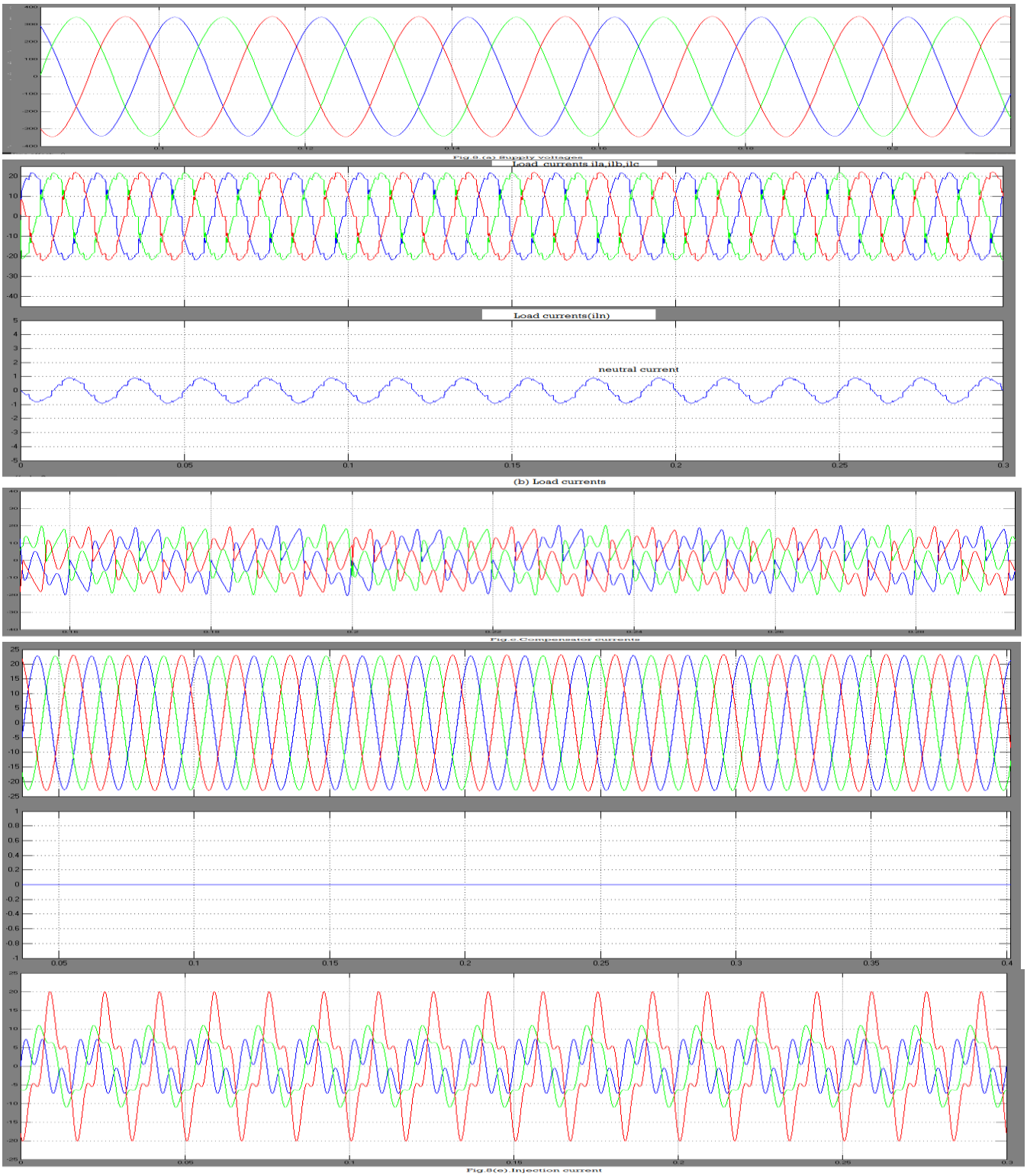


Figure 8 (a) Supply Voltages. (b) Load currents (c) Compensator currents. (d) Source currents after compensation (e) injection current :-

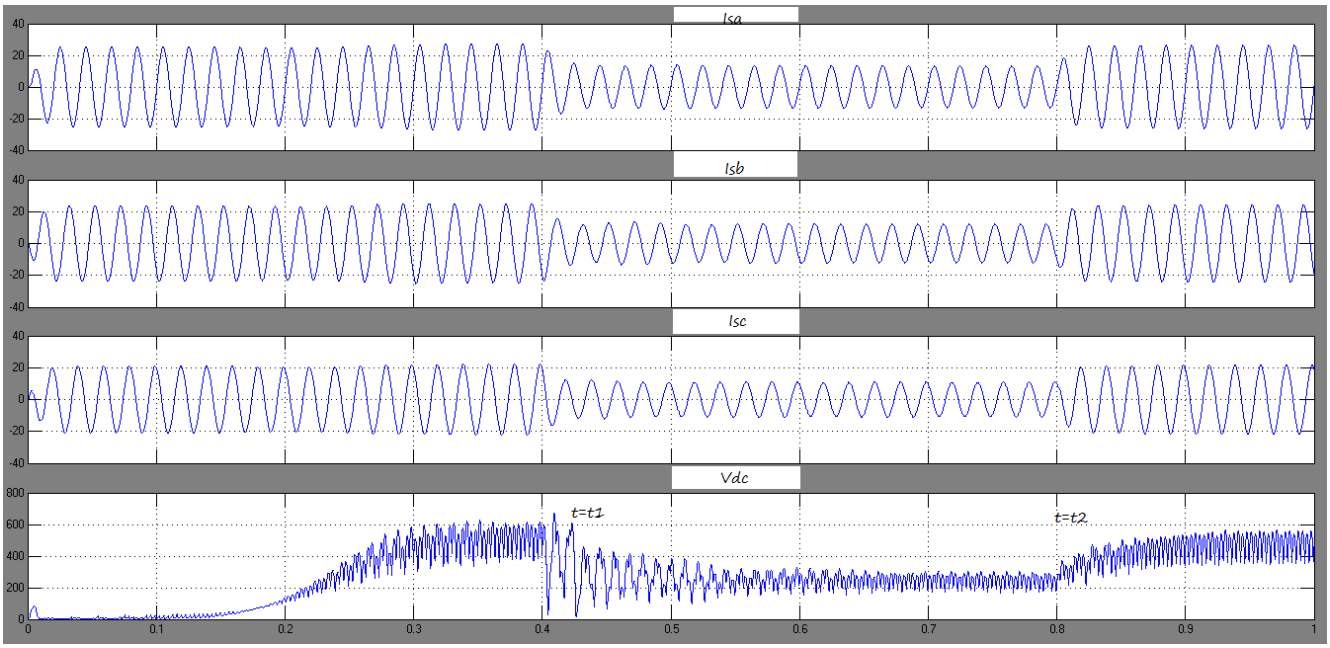


Figure 9:-Source currents and dc-link voltage with a conventional dc-link voltage controller.

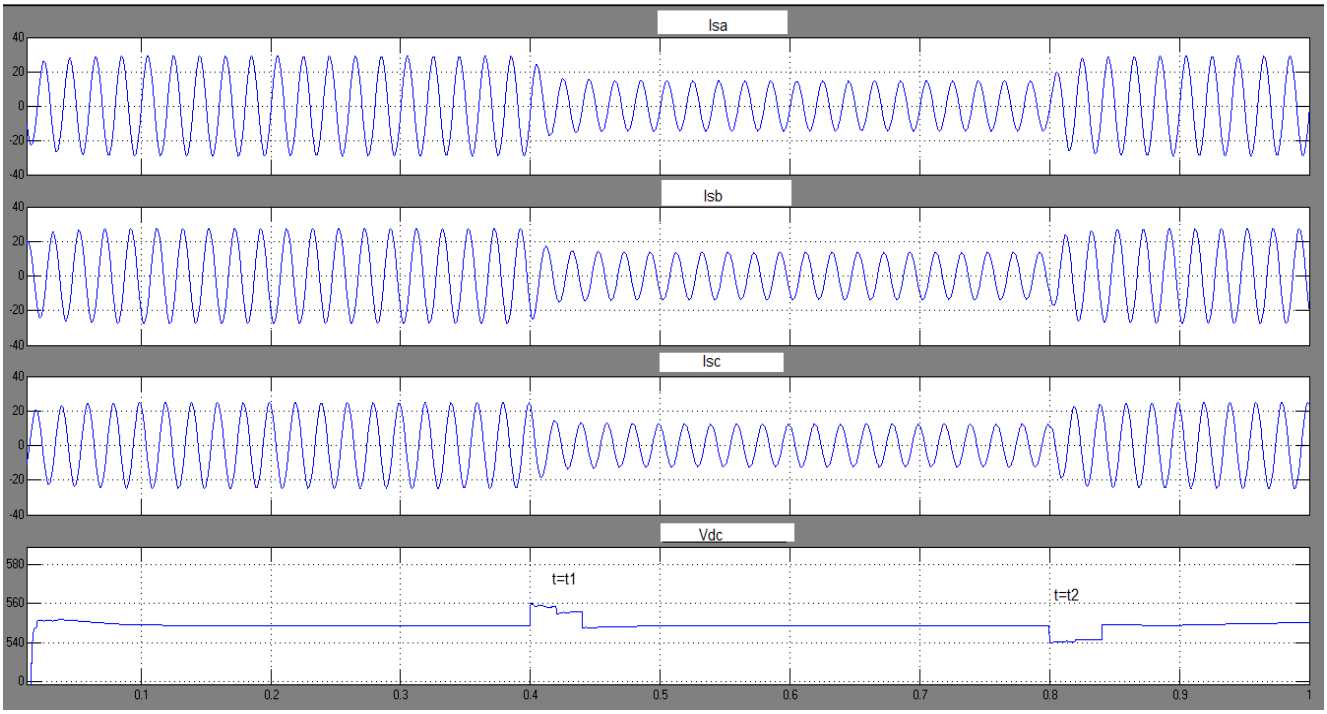


Figure 10:- Source currents and dc-link voltage with a fast-acting dc-link voltage controller

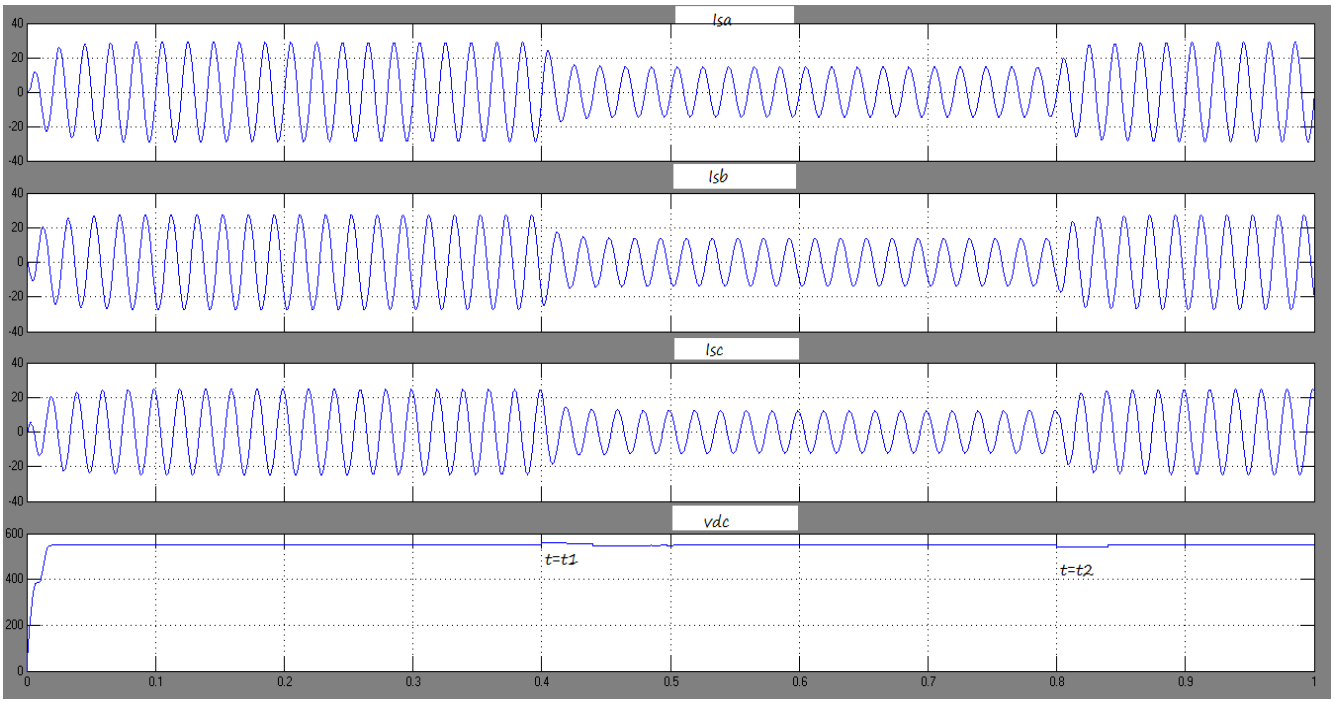


Fig.11. source currents and DC-link voltage with a fast Acting DC-link voltage controller and proposed VSI controller using PQ-theory

X. CONCLUSION

A VSI topology for DSTATCOM compensating ac unbalanced and nonlinear loads and a dc load supplied by the dc link of the compensator is presented. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. The energy based fast acting dc link voltage controller is suggested to ensure the fast transient response of the compensator. Mathematical equations are developed to compute the gains of this controller. The efficacy of the proposed controller over the conventional dc link voltage controller and PQ-theory are established through the digital simulation studies. It is observed from these studies that the proposed dc link voltage controller gives fast transient response under load transients and PQ-theory.

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